REMARKS

Status of the Claims

Claims 1-5 are now present in this application. Claim 1 is independent. No amendments have been made by way of the present submission, thus, no new matter has been added. Further, no new issues have been raised, which present the burden of additional search and/or consideration.

In view of the following remarks, the Examiner is respectfully requested to withdraw all rejections and allow the currently pending claims.

Issue under 35 U.S.C. § 103

Claims 1-5 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Davis et al., US 6,257,760 ("Davis") in view of Yoon et al., US 2003/0077870 ("Yoon"). This rejection is respectfully traversed.

The Present Invention and its Advantages

Independent claim 1 relates to a vapor phase growth method for growing an epitaxial layer on a semiconductor substrate, comprising:

measuring a resistivity of arbitrary semiconductor substrates at a room temperature;

obtaining respectively a relationship between a heating temperature and a temperature of a surface of the arbitrary semiconductor substrates, for the arbitrary semiconductor substrates having different resistivities;

setting and adjusting said heating temperature of a semiconductor substrate to be used based on (i) a measured resistivity of the semiconductor substrate to be used and (ii) the obtained relationship between the heating temperature and the temperature of the surface of said semiconductor substrate; and

growing the epitaxial layer, wherein the temperature of said surface of said semiconductor substrate to be used is indirectly controlled by adjusting said heating temperature.

The present invention was made on the basis of the following findings:

(1) Each substrate has its own resistivity at room temperature. In particular, even when substrates share the same ingot, the substrates cut out from the same ingot are different in

their resistivity in small amounts at room temperature when the cutting positions thereof vary with each other (refer to FIG. 2).

(2) When the substrates differ in their resistivity at room temperature, the degree of surface temperature rise of the substrates is to be different. In this instance, the temperature rise is caused by receiving heat from the apparatus (e.g. MBE apparatus) at the time of the epitaxial growth. In other words, the thermal difference to be generated between the heating temperature which is set for the apparatus and the actual surface temperature of the substrates depends on the difference in the resistivities at room temperature of the substrates. Thus, substrates having the same resistivity at the room temperature share the same thermal difference between the heating temperature and the actual surface temperature of the substrates.

Based on the above described findings, in order to obtain the desired degree of the actual surface temperature of the substrates, the present invention discloses the following configuration. That is, as required in independent claim 1:

1. the resistivity of arbitrary semiconductor substrates at a room temperature is previously measured;

2. the relationship between the heating temperature and the temperature of the substrate surface is obtained, for each of the arbitrary semiconductor substrates having different resistivities;

3. the heating temperature is set and adjusted based on (i) the measured resistivity of the semiconductor substrate to be used and (ii)the above mentioned obtained relationship.

According to this configuration, the heating temperature indicated, for example, by a thermocouple, and the like, can be adjusted in accordance with the difference of the substrates (the difference in their resistivity at the room temperature), based on the thermal difference to be generated between the heating temperature and the actual surface temperature of the substrates. Thereby, the surface temperature of the substrate can be controlled accurately so as to be a desired temperature. Thus, an epitaxial layer having a stable quality can be grown with superior reproducibility, and a semiconductor element having superior characteristic can be stably manufactured (see paragraph [0016] of the specification).

Distinctions Between the Present Invention and the Cited Art

The Examiner asserts in the Office Action that the configurations defined in claim 1 are

mainly taught by Davis, and that the present invention will be necessarily be arrived at by the combination with Yoon which teaches the vapor phase method for growing an epitaxial layer. However, Applicants respectfully disagree with the Examiner. In fact, there are several deficiencies in the stated rejection and therefore, there exists no *prima facie* case of obviousness, as discussed below.

First, Applicants submit that the Examiner has not provided either specific motivation or a rationale to combine the two references. Indeed, Applicants submit that, absent hindsight, no such motivation or rationale exists. For example, Yoon discloses a method to reduce parasitic capacitance in an InP/InGaAs DHST by selective wet etching. However, Yoon does not disclose any details regarding a vapor phase growth method, much less any indication for an accurate temperature control. Accordingly, there appears to be neither motivation nor rationale to modify the cited references or to combine the reference teachings.

Indeed, Applicants submit that it is only with the benefit of hindsight that the Examiner may combine these references. However, one of skill in the art has no such benefit. In fact, the Examiner's rejection amounts to no more than an "obvious to try" style rejection, which as explained below, falls within an impermissible category of obvious to try. The issue of "obvious to try was revisited by the Federal Circuit in In re Kubin (2008-1184, decided April 3, 2009). The court highlighted an earlier decision of In re O'Farrell, 853 F.2d 894 (Fed. Cir. 1988), where it was cautioned that "obvious to try" is an incantation whose meaning is often misunderstood:

> It is true that this court and its predecessors have repeatedly emphasized that "obvious to try" is not the standard under § 103. However, the meaning of this maxim is sometimes lost. Any invention that would in fact have been obvious under § 103 would also have been, in a sense, obvious to try. The question is: when is an invention that was obvious to try nevertheless nonobvious?

In re O'Farrell, 853 F.2d 894, 903 (Fed. Cir. 1988).

The Federal Circuit held in In re Kubin that to differentiate between proper and improper applications of "obvious to try," it is necessary to understand two classes of situations where "obvious to try" is erroneously equated with obviousness under § 103. In the first class of cases,

> what would have been "obvious to try" would have been to vary all parameters or try each of numerous possible choices until one possibly arrived at a successful result, where the prior art gave either no indication of which parameters were critical or no direction as to which of many possible choices is likely to be successful.

Id. In such circumstances, where a defendant merely throws metaphorical darts at a board filled with combinatorial prior art possibilities, courts should not succumb to hindsight claims of obviousness. The inverse of this proposition is succinctly encapsulated by the Supreme Court's statement in KSR that where a skilled artisan merely pursues "known options" from a "finite number of identified, predictable solutions," obviousness under § 103 arises. 550 U.S. at 421.

> The second class of O'Farrell's impermissible "obvious to try" situations occurs where what was "obvious to try" was to explore a new technology or general approach that seemed to be a promising field of experimentation, where the prior art gave only general guidance as to the particular form of the claimed invention or how to achieve it.

853 F.2d at 903. Again, KSR affirmed the logical inverse of this statement by stating that § 103 bars patentability unless "the improvement is more than the predictable use of prior art elements according to their established functions." 550 U.S. at 417.

In the present instance, Applicants submit that the Examiner has participated in impermissible "obvious to try" analysis. As such, Applicants submit that the outstanding rejection is improper and must be withdrawn.

Second, even if the references are combined, the present invention cannot be arrived at therefrom. For instance, Davis discloses that Al and Si layers having superlattice structures are deposited on a Si substrate; each of the superlattice structures is annealed; and the resistivity of each of the superlatice structures, which has been cooled down, is measured. However, the Al and Si layers taught in Davis do not form single crystals. Further, what is disclosed in Davis is based on the resistivity variation caused by the alloying process. Moreover, it is shown in step 44 of FIG. 3 that Davis requires another superlattice structure to be formed, the substrate which is subjected to the measurement in step 42 can no longer be used in the following process. This means that the process temperature determined in step 48 is based upon the calibration curve obtained by the sacrifice of another substrate shown in steps 40 and 42.

On the other hand, the present invention provides a method to obtain the appropriate substrate temperature based upon its own resistivity that the substrate to be subjected to the heating process originally has.

Davis, Yoon, and/or the combination thereof fails to even mention the variation in surface temperature generated in heating process, deriving from the resistivity difference that the

substrate originally has, thereby the temperature control cannot be performed with reproducibility and with perfection as in the present invention.

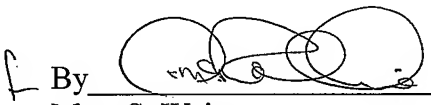
In view of the foregoing, since the configurations defined in the vapor phase growth method as claimed are not at all taught by the combination of the cited references, the results to be achieved as described above cannot be obtained from the prior art. As such, it is believed the present claims are patentable over the cited references, and the present application now stands in condition for allowance.

Should there by an outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Linda T. Parker, Registration No. 46,046, at the telephone number of the undersigned below to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Director is hereby authorized in this, concurrent, and future replies to charge any fees required during the pendency of the above-identified application or credit any overpayment to Deposit Account No. 02-2448.

Dated: MAR 22 2010

Respectfully submitted,



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